CLAIMS

1. An apparatus, comprising:

a searcher for correlating a received signal with a synchronization sequence to produce a first plurality of search results, each search result comprising at least one of an energy indicator or an offset; and

a processor for comparing a stored offset with the offset of a search result of the first plurality of search results and removing the corresponding search result from the first plurality of search results when the search result offset is within a pre-determined threshold of the stored offset.

2. The apparatus of claim 1, further comprising a memory for storing a first plurality of scrambling code identifiers and associated offsets, the stored offset selected therefrom.

3. The apparatus of claim 1, further comprising a receiver for receiving a signal from a base station to generating the received signal therefrom.

4. The apparatus of claim 1, wherein the received signal comprises a scrambling code transmitted over a plurality of slots and a synchronization sequence repeated during each slot.

5. The apparatus of claim 4, wherein the processor further adds an integer multiple of the number of chips in a slot to the search result prior to comparing.

6. The apparatus of claim 4, wherein the processor further adds an integer multiple of the number of chips in a slot to the stored offset prior to comparing.

7. The apparatus of claim 1, wherein the searcher further correlates the received signal with a scrambling code over a search window to produce a list search result.

8. The apparatus of claim 1, wherein:

the memory further stores a second plurality of scrambling code identifiers;

the searcher further correlates the received signal with a scrambling code over a search window to produce a list search result; and

the processor further directs the searcher to search a search window around the offset associated with one or more of the first plurality of search results using one or more scrambling codes identified by one or more of the second plurality of scrambling code identifiers, respectively.

9. The apparatus of claim 8, wherein the processor further removes a scrambling code identifier from the second plurality of scrambling code identifiers when the list search result exceeds a pre-determined threshold.

10. The apparatus of claim 8, wherein the second plurality of code identifiers corresponds to undetected neighbor cells.

11. The apparatus of claim 8, wherein the first plurality of code identifiers corresponds to previously identified cells.

12. The apparatus of claim 1, wherein the pre-determined threshold is a fixed number of chips.

13. The apparatus of claim 1, wherein the pre-determined threshold is variable, increasing with an increase in the time lapsed since the associated offset was determined.

14. The apparatus of claim 4, wherein the received signal further comprises a secondary synchronization sequence comprising a series of sub-sequences in the corresponding series of slots, the secondary synchronization sequences identifying the frame timing and a unique subset of scrambling codes.

15. The apparatus of claim 14, wherein the searcher further:

correlates the received signal with the sub-sequences in accordance with the offset of one of the first plurality of search results to identify the respective secondary synchronization sequence;

correlates the received signal with each of the subset of scrambling codes until the correlation energy exceeds a threshold; and

generates an indicator identifying the scrambling code transmitted at the offset of the search result of the first plurality of search results.

16. A method of searching, comprising:

correlating a received signal with a synchronization sequence to produce a plurality of search results;

comparing a stored offset with the offset of one of the plurality of search results; and

removing the search result from the plurality of search results when its offset is within a pre-determined threshold of the stored offset.

17. The method of claim 16, further comprising selecting the stored offset from a plurality of scrambling code identifiers and associated offsets stored in a memory.

18. The method of claim 16, further comprising correlating the received signal with a scrambling code over a search window to produce a list search result.

19. The method of claim 18, wherein the scrambling code is selected from a neighbor list.

20. An apparatus, comprising:

means for correlating a received signal with a synchronization sequence to produce a plurality of search results;

means for comparing a stored offset with the offset of one of the plurality of search results; and

means for removing the search result from the plurality of search results when its offset is within a pre-determined threshold of the stored offset.

21. Processor readable media operable to perform the following steps:

correlating a received signal with a synchronization sequence to produce a plurality of search results;

comparing a stored offset with the offset of one of the plurality of search results; and

removing the search result from the plurality of search results when its offset is within a pre-determined threshold of the stored offset.